REMARKS

The Office Action dated March 15, 2002 has been carefully considered. In response to the restriction requirement included in that Office Action, the applicant hereby affirms the provisional election made by the applicant's representative, Francis E. Morris, on March 6, 2002, without traverse, to prosecute the invention of Group 1, claims 1 - 15.

Claims 1 through 8 have been canceled without prejudice. Claim 9 has been amended and a new claim 20 has been added. Accordingly, reconsideration of this application, as amended, and allowance are respectfully requested.

Claims 1-2, 4-7, 9, 11-14 have been rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,294,831 to Shishido *et al.* ("Shishido"). The Examiner cites the semiconductor carrier illustrated in Figure 2 of Shishido as anticipating claims 1-2, 4-7, 9, 11-14. This rejection is respectfully traversed.

Claims 1-2, and 4-7 have been canceled without prejudice.

As amended, independent claim 9 recites a primary substrate, "a metal heat sink plate, whose thermal coefficient of expansion is substantially different from that of said primary substrate" and a supplemental substrate wherein "the presence of the supplemental substrate prevents the semiconductor chip carrier from warping." The metal heat sink plate contacts the primary substrate on one side and the supplemental substrate on its opposing side. As described in the specification of the present application, for example, at page 2, lines 20-26 and page 4, lines 1-6, the present invention utilizes the supplemental substrate, which has a substantially similar coefficient of thermal expansion as the primary substrate, to counter balance the bending force resulting from the mismatch of coefficients of thermal expansion between the primary substrate and the metal heat sink plate. Thus, this invention provides a solution to the chip-carrier warping problem where the coefficient of thermal expansion of the metal heat sink plate cannot be matched with that of the primary substrate.

In contrast, Figure 2 of Shishido discloses a semiconductor chip carrier having a substrate **12** and a metal structure **30** (of parts **30a** and **30b**) bonded to the substrate **12.** Both parts **30a** and **30b** of structure **30** have the same coefficient of thermal expansion as the

substrate **12** so the resulting package **32** does not warp. (Shishido at column 4, lines 3-12). Thus, Shishido does not teach a solution to the situation where the coefficient of thermal expansion of the metal heat sink plate is substantially different than the coefficient of thermal expansion of the substrate **12.**

Therefore, Shishido does not show or suggest the provision of a supplemental substrate as recited in claim 9 as amended. Accordingly, allowance of claim 9 over Shishido is respectfully requested.

Claims 11-14 depend from claim 9, which is allowable over Shishido. Accordingly, claims 11-14 should also be allowed over Shishido and their allowance is respectfully requested.

Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Shishido. This rejection is respectfully traversed.

Claim 10 depends from claim 9, which is allowable over Shishido. Accordingly, claim 10 should also be allowed over Shishido and its allowance is respectfully requested.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shishido and further in view of United States Patent No. 6,288,900 to Johnson *et al.* ("Johnson"). Johnson was cited for its disclosure in Figure 6 of a supplemental substrate 29 having a cavity that exposes a portion of metal heat sink plate 28. This rejection is respectfully traversed because these references cannot be combined. As noted above, Shishido teaches that the substrate and the various parts of the metal structure all have the same coefficient of thermal expansion (CTE). Johnson, however, teaches that at least plate 28 and substrate 29 comprise different materials (Col. 4, line 11) allowing for adjustment of both stiffness and CTE (Col. 4, lines 4-5). Since the two references teach incompatible structures, they cannot be combined.

Claim 15 depends from claim 9, which is allowable over Shishido. Accordingly, claim 15 should also be allowed over Shishido in view of Johnson. Allowance of claim 15 is, thus, respectfully requested.

New dependent claim 20 has been added to further define the semiconductor chip carrier of claim 9 as disclosed in the present application. The subject matter recited in the new claim is fully supported by the originally-filed disclosure of the present application. Support for new claim 20 can be found, for example, in Figure 1 and the text on page 3, lines 29-30, of the present application. Figure 1 illustrates substrate **32** having a hole forming a die-attach cavity **38** wherein semiconductor die **40** is attached to the metal heat sink plate **34.**

After entry of this amendment, the pending claims are: Claims 9-15, and the new claim 20.

For the above reasons, the rejection of claims 9-15 over the prior art should be withdrawn and these claims, along with new claim 20, should be allowed. Reconsideration, entry of the above amendments, and allowance are respectfully requested. Please charge any fees due for the submission of this response to Pennie & Edmonds LLP deposit account No. 16-1150.

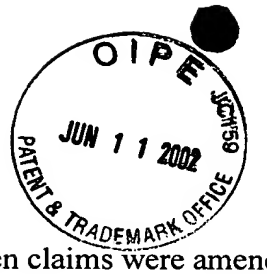
Respectfully submitted,

Date June 11, 2002

Francis E. Morris

Francis E. Morris (Reg. No. 24,615)
By: Won Joon Kouh (Reg. No. 42,763)
PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, New York 10036-2711
(212) 790-9090

Enclosure



APPENDIX

Changes to the Claims

The rewritten claims were amended as follows:

9. (Amended) A semiconductor chip carrier comprising:

a primary substrate;

a metal heat sink plate, whose thermal coefficient of expansion is substantially different from that of said primary substrate, having a first side and an opposing second side where said primary substrate is attached to said first side; and

a supplemental substrate being attached to said second side of said metal heat sink plate, wherein said supplemental substrate is constructed from a material having a substantially similar coefficient of thermal expansion as that of said primary substrate so that the presence of the supplemental substrate prevents the semiconductor chip carrier from warping.

10. A semiconductor chip carrier according to claim 9, wherein said supplemental substrate is constructed from a same material as said primary substrate.

11. A semiconductor chip carrier according to claim 9, wherein said primary substrate is constructed from a material selected from one of Bis-malesimide triazine epoxy, FR4, polyimide, and polytetrafluoroethylene.

12. A semiconductor chip carrier according to claim 9, wherein said chip carrier is a ball-grid array chip carrier.

13. A semiconductor chip carrier according to claim 9, wherein said metal heat sink plate consists of a metal selected from one of Cu, Cu-W, Al, and alloys thereof.

14. A semiconductor chip carrier according to claim 9, wherein said supplemental substrate has a Cu-Ni finish layer.

15. A semiconductor chip carrier according to claim 9, wherein said supplemental substrate has a cavity exposing a portion of said metal heat sink plate.

20. (New) A semiconductor chip carrier according to claim 9, wherein said primary substrate comprises a hole forming a die-attach cavity wherein the semiconductor chip is attached to the first side of the metal heat sink plate within the die-attach cavity;